In the Claims

1. (Currently amended) A circuit for deterministic testing of edge-triggered logic, comprising:

~~An digital circuit having~~ at least first and second edge-triggered devices, each being clocked by a respective clock signal~~respectively receiving first and second clock signals, and~~

a selectable circuit path for forming ~~at least one~~a scan data path that includes the first and second edge-triggered devices~~, including:~~; and

a latch in the scan data path, the latch having ~~a data~~ an input coupled to ~~receive~~ an output ~~from~~ of the first edge-triggered device and an output coupled to an input of the second edge-triggered device, the latch being clocked by ~~the second~~ a test-clock signal to temporarily hold data previously held by the first edge-triggered device while the first and second edge-triggered devices change state.

2. (Currently amended) The ~~digital~~ circuit of claim 1, ~~including~~ further comprising multiplexer circuits for selectively forming the scan data path in response to a scan test signal.

3. (Currently amended) The ~~digital~~ circuit of claim 2, wherein the first and second edge-triggered devices form functional circuits in the absence of the scan test signal.

4. (Currently amended) The ~~digital~~ circuit of claim 1, wherein the ~~first and second~~ test-clock signal is clocked in synchronism relative to the respective clock signals but in phase relative thereto that accounts for data transfer through the latch ~~are asynchronous to one another~~.

5. (Currently amended) A digital circuit structured ~~to be subjected to~~for deterministic testing of edge-triggered logic ~~scan testing~~, comprising:

a scan data input;

a scan data output;

at least first and second clock domains each including one or more edge-triggered devices, each clock domain receiving first and second clock signals;

a data path selectable in response to a scan test signal for forming a scan data path between the scan data input and the scan data output that includes the first and second clock domains with a scan data path portion from an output of the first ~~devices~~ edge-triggered device to an ~~output~~ input of the second edge-triggered device; and

a latch in the scan data path portion that is clocked by the second clock signal.

6. (Currently amended) A method ~~of scan testing~~for deterministic testing of digital logic ~~comprising~~ with as least first and second digital circuits ~~having a data path from one to the other and~~that are respectively clocked by first and second clock signals, each digital circuit including at least one edge-triggered device, the method ~~including the steps of~~comprising:

providing a latch element in the data path clocked by a test clock;

asserting a scan test signal to cause at least one serial scan chain to be formed that includes the first and second digital circuits on a scan data path;

operating the first, second, and test clock signals to cause the scan chain to receive test data such that the test clock assumes one state ~~to hold~~causing the latch element to hold its state while the edge-triggered devices are caused to change state by the first and second clock signals and such that the test clock then assumes a second state to allow data to pass along the ~~test~~ scan data path from the ~~one~~ first digital circuit to the ~~other~~second.

7. (New) A circuit for deterministic testing of edge-triggered logic, comprising:

a first edge-triggered device having a data input and a data output, and configured to transfer data from input to output by a logic transition of a first clock;

a second edge-triggered device having a data input and a data output, and configured to transfer data from input to output by a logic transition of a second clock; and

a latch interposed between the output of the first device and the input of the second device and having a latch clock input which in a first state causes the latch to hold data captured from the first edge-triggered device steady even while the first edge-triggered device experiences a state transition and which in a second state causes the latch to allow the data to follow any state transition of the first device.

8. (New) A circuit as recited in claim 7 wherein the first and second edge-triggered devices include

a multiplexer having a plurality of muliplexer data inputs, a multiplexer data output, and a data selection input for selecting one of the multiplexer data inputs in response to a test signal, and

an edge-triggered flip-flop having a clock input, a flip-flop data output, and a flip-flop data input connected to the multiplexer data output,

wherein data transfer from one of the plurality of multiplexer data inputs to the flip-flop data output is triggered by a logic transition of a signal at the clock input.

9. (New) A method for deterministic testing of edge-triggered logic, the method comprising:

setting a test signal in a test state so as to form a first scan chain that is responsive to a logic transition of a first clock signal and a second scan chain that is responsive to a logic transition of a second clock signal, the first and second scan chains each having an input for receiving scan data and an output for respectively providing the scan data; and

operating a third clock to control a latch interposed between the output of the first scan chain and the input of the second scan chain causing the latch to experience a hold state or a follow state, the hold state being experienced during a time period prior to the logic transition of the first clock signal and subsequent to the logic transition of the second clock signal such that data present at the output of the first scan chain prior to the logic transition of the first clock signal is held in the latch until after the logic transition of the second clock, the follow state being experienced outside the time period.